REMARKS

In the Office Action, the Examiner noted that claims 13-16 and 18-24 are pending in the application and that claims 13-16 and 18-24 are rejected. Claims 1-12 and 17 have been withdrawn from consideration. By this response, claims 13 and 19 are amended and claim 14 is cancelled. In view of the above amendments and the following discussion, the Applicant submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. REJECTION OF CLAIMS UNDER 35 U.S.C. §102(e)

The Examiner rejected claims 13 and 19 as being anticipated by Sinclair et al. (U.S. Patent 6,711,059, issued March 23, 2004) ("Sinclair"). The rejection is respectfully traversed.

A. Claim 13

More specifically, the Applicant has amended claim 13 to incorporate the features of claim 14, and claim 14 has been cancelled. As such, Applicants' claim 13 recites that the at least one memory resource is configured by storing data at a location associated with a reset vector of the processor. The Applicant addresses the rejection of claim 14 (the subject matter of which is now in claim 13) for obviousness below.

Sinclair teaches loading one or more sectors of boot firmware code from a Flash memory to SRAM while a processor is halted. (Sinclair, col. 5, lines 18-30). There is no teaching or suggestion in Sinclair that the boot firmware code is stored at a location associated with a reset vector of the processor. The Examiner conceded that Sinclair does not explicitly disclose such a feature. (Office Action, p. 3).

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Sinclair does not teach configuring at least one memory

resource by storing data at a location associated with a reset vector of the processor while the processor is halted, Sinclair does not teach each and every element of claim 13. Accordingly, the Applicant contends that claim 13 is not anticipated by Sinclair and, as such, fully satisfies the requirements of 35 U.S.C. §102.

B. Claim 19

The Examiner stated that Sinclair teaches maintaining a processor in a halt condition, stopping an execution cycle of the processor, releasing the processor from the halt condition, configuring a memory resource, and starting the execution cycle of the processor. (Office Action, pp. 2-3). The Examiner asserted that Sinclair inherently teaches stopping the execution cycle given that a processor is being initialized. The Examiner further asserted that Sinclair inherently teaches starting the execution cycle of the processor given that the processor executes code. (Office Action, p. 3).

The Applicant has amended claim 19 to clarify the order in which the steps are performed. Namely, when the processor is released from the halt condition, the execution cycle remains stopped. Moreover, the at least one memory resource is configured after the processor is released from the halt condition and while the execution cycle of the processor is stopped. Support for the amendment is found in paragraphs 0050 and 0051 of Applicant's specification.

Sinclair does not teach or suggest Applicant's invention recited in claim 19 as arranged therein. In particular, Sinclair does not teach or suggest releasing the processor from the halt condition, but maintaining a stop of the execution cycle. The fact that the execution cycle of the processor is stopped while the processor is halted does not teach or suggest maintaining a stop of the execution cycle after releasing the processor from the halt condition. Sinclair also fails to teach or suggest configuring at least one memory resource after the processor is released from the halt condition and while the execution cycle of the processor is stopped. In Sinclair, the SRAM is configured when the processor is halted or while the processor is operating. There is no teaching or suggestion that the SRAM is configured after the processor has been released from halt, but while the processor execution cycle is stopped.

Accordingly, the Applicant contends that claim 19 is not anticipated by Sinclair

and, as such, fully satisfies the requirements of 35 U.S.C. §102.

II. REJECTION OF CLAIMS 14-16, 18, 20-24 UNDER 35 U.S.C. §103(a)

The Examiner rejected claims 14-16, 18, and 20-24 are rejected as being unpatentable over Sinclair in view of Spiegel et al (U.S. Patent 6,711,675, issued March 23, 2004) ("Spiegel"). The rejection is respectfully traversed.

A. Claims 14-16

The Applicant has cancelled claim 14 and incorporated its features into claim 13. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicant's invention recited in claim 13. Namely, the combination of Sinclair and Spiegel does not teach or suggest configuring at least one memory resource by storing data at a location associated with a reset vector of the processor while the processor is halted. The deficiency of Sinclair with respect to teaching or suggesting such feature is detailed above.

Spiegel teaches a protected boot sequence in a computer system. (See Spiegel, Abstract). In particular, when a computer system boots, a system reset vector is invoked, which directs the processor to begin execution at a specific address within a firmware hub. The firmware hub is a nonvolatile memory block containing instructions that validate the boot sequence. (Spiegel, col. 2, lines 9-25). Spiegel does not teach or suggest storing data at a memory location associated with a reset vector of the processor. As disclosed in Spiegel, the firmware hub pointed to by the system reset vector is nonvolatile memory. There is no teaching or suggestion in Spiegel of a step of storing data in the firmware hub, in particular, storing data at a location associated with the system reset vector. Rather, Spiegel assumes that the firmware hub already includes the control code.

As discussed above, Sinclair teaches a system that loads one or sectors of boot firmware code from a Flash memory to SRAM while a processor is halted. The system reset vector approach of Spiegel does not fit within the system of Sinclair. Specifically, Sinclair requires that firmware code be loaded into the SRAM while the processor is halted. In Spiegel, no data is loaded into the firmware hub pointed to by the system

reset vector. The only conceivable combination of Sinclair and Spiegel results in a reset vector of the processor in Sinclair pointing to some nonvolatile memory, such as the Flash memory. Sinclair, however, does teach or suggest a step of storing data in the Flash memory while the processor is halted.

As such, Applicant's invention of claim 13 is nonobvious in view of the combination of Sinclair and Spiegel. Claims 15 and 16 are amended to expressly depend from Claim 13. Claims 15-16 and 18 depend from claim 13 and recite additional features therefor. Since the cited combination does not render obvious Applicant's invention of claim 13, claims 15-16 and 18 are also nonobvious. Accordingly, the Applicant contends that claims 13, 15-16, and 18 are patentable over the combination of Sinclair and Spiegel and, as such, fully satisfies the requirements of 35 U.S.C. §103.

B. Claims 20-24

Claims 20-24 depend from claim 19 and recite additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicant's invention recited in claim 19. Namely, the combination of Sinclair and Spiegel does not teach or suggest (1) releasing the processor from the halt condition, but maintaining a stop of the execution cycle; and (2) configuring at least one memory resource after the processor is released from the halt condition and while the execution cycle of the processor is stopped. The deficiency of Sinclair with respect to teaching or suggesting such feature is detailed above. Spiegel generally teaches invoking a system reset vector that directs a processor to begin execution at a specific address in a firmware hub. Spiegel is devoid of any teaching or suggestion of releasing the processor from the halt condition, but maintaining a stop of the execution cycle. Spiegel is also devoid of any teaching or suggestion of configuring a memory resource after the processor has been released from halt, but while the processor execution cycle is stopped.

As such, no conceivable combination of Sinclair and Spiegel renders obvious Applicant's invention of claim 19. Accordingly, the Applicant contends that claims 20-24, which depend from claim 19, are patentable over the cited combination and, as

such, fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, the Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Michael R. Hardaway at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 06, 2006.

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Signature